CPDA-02 Digital + Analog Processor

A Much Better Idea : Logical : Unique

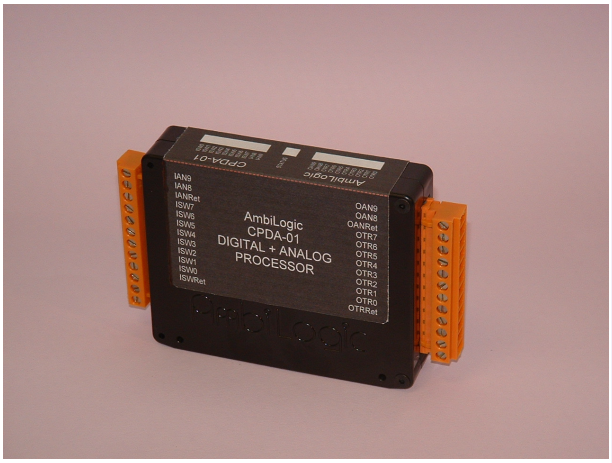
AmbiLogique

Electronic Controllers

Features:-

20 inputs and outputs:-

- 8: digital inputs
- 2: 0-1V analogue inputs
- 8: NPN transistor outputs
- 2: 0-10V analogue outputs.



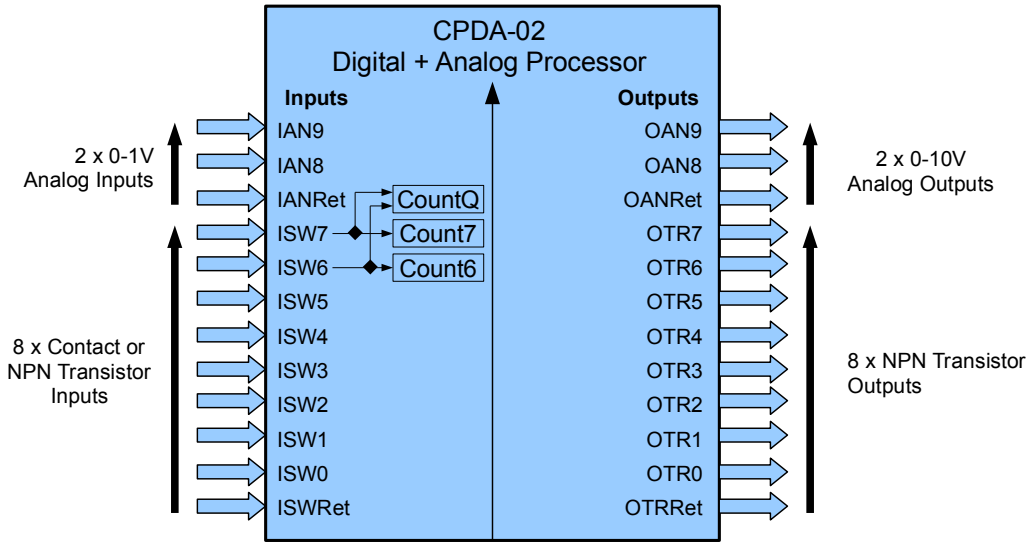
3 Medium-Speed (1kHz) counters

- 2 up-count
- 1 quadrature up/down-count

Easy Function Block Programming
Fast 16 Hz Scan Rate
Low 2W Power Consumption.
Large 800 Function Block Capacity

Connections via detachable screw terminals.

Built-in Serial Communication Port
50 Computer Interface Registers (16 for firmware earlier than 2.00)
All Internal Signals Viewable via Serial Port
Backplane Communications Error Logging
K-Factor Area for Semi-permanent Constants



Count6, Count7 = up counters; CountQ = quadrature up/down counter.

Connection Diagram

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CPDA-02 Digital + Analog Processor

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Electronic Controllers

The CPDA-02 is a programmable digital + analogue controller which plugs into and controls an AmbiLogique backplane. This is a non-networked controller designed for stand-alone operations.
The CPDA-02 replaces the CPDA-01 and offers more Function Blocks, together with the new K-Factors memory area.
Expansion modules can be added to the backplane, or can be connected via a screened cable for distributed control.

The CPDA-02 has the following selection of inputs and outputs built in:-

- 8 switch or NPN non-isolated transistor digital inputs
- 2 0 to 1V non-isolated analogue inputs
- 8 NPN transistor non-isolated digital outputs (these can drive relays)
- 2 0 to 10 V non-isolated analogue outputs.

This makes a total of 20 inputs and outputs.

Connections are made via detachable screw terminals.

The CPDA-02 controller plugs into the Controller slot in any of the AmbiLogique backplanes, and takes its power from the backplane. The control diagram which determines the PLC behaviour is loaded in the CPDA-02.

Expansion modules can be plugged into any numbered slot of the backplane, and automatically pick up their slot address from the backplane. When a facility in an expansion module is referenced in the control diagram, the CPDA-02 automatically implements the communications protocols necessary to gather input information from the expansion module or to send output commands to the module.

Each backplane transaction is counted and the count maintained in an internal register. If an error is detected, the error is logged and categorised. The total transaction count and the error counts may be inspected via the RS-232 serial port.

Programming is carried out on a Windows ® personal computer (PC) on which the AmbiLogique design software AmbiL_PLC.exe is run. This software also runs on Linux computers equipped with CrossOver and Mac® computers with CrossOver or Parallels.
AmbiL_PLC enables you to construct a function-block-based diagram which defines the program which the CPDA-02 will run in service.
The PC is then connected to the CPDA-02 via a serial RS-232 cable, and the compiled diagram is uploaded into the CPDA-02.
Whilst in operation, the state of the internal signals in the CPDA-02 can be displayed on the diagram on the PC screen.
Once the program has been tested, the PC can be disconnected, and the CPDA-02 will continue to operate independently.

The new K-Factors area provides a means of editing only the constants in a control diagram. In earlier PLC's, changing the value of a constant meant that the entire control diagram needed to be re-loaded into the PLC, because the location of the constants might be changed as a result of a change in value. The new K-Factor area allows you, the programmer, to determine the location of each constant: a new software facility allows you to inspect these K-Factors, edit them, and re-load them into the PLC without the need to re-load the control diagram.

The CPDA-02 will run control diagrams developed for the CPDA-01 processor without modification.
The CPDA-02 is also plug compatible with the CPDA-01 and may be directly substituted for the earlier model.
However, the CPDA-02 offers a control diagram space three times the size of the CPDA-01, and the new facility of editable K-Factors.

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Connections:

Note: The Subslot, Register and Mask values are needed to map the physical inputs and outputs into the Control Diagram.

Terminal	Signal	Description	Subslot	Register	Mask
A12	IAN9+	Analogue Input	0	3	0
A11	IAN8+	Analogue Input	0	2	0
A10	IANRet	Return for Analogue Inputs			
A09	ISW7+	Switch / Contact / NPN Input	0	1	128
A08	ISW6+	Switch / Contact / NPN Input	0	1	64
A07	ISW5+	Switch / Contact / NPN Input	0	1	32
A06	ISW4+	Switch / Contact / NPN Input	0	1	16
A05	ISW3+	Switch / Contact / NPN Input	0	1	8
A04	ISW2+	Switch / Contact / NPN Input	0	1	4
A03	ISW1+	Switch / Contact / NPN Input	0	1	2
A02	ISW0+	Switch / Contact / NPN Input	0	1	1
A01	ISWRet	Return for ISW Inputs			
C01	OAN9+	0-10 V Analogue Output	0	6	0
C02	OAN8+	0-10 V Analogue Output	0	5	0
C03	OANRet	Return for Analogue Outputs			
C04	OTR7+	Transistor Output	0	4	128
C05	OTR6+	Transistor Output	0	4	64
C06	OTR5+	Transistor Output	0	4	32
C07	OTR4+	Transistor Output	0	4	16
C08	OTR3+	Transistor Output	0	4	8
C09	OTR2+	Transistor Output	0	4	4
C10	OTR1+	Transistor Output	0	4	2
C11	OTR0+	Transistor Output	0	4	1
C12	OTRRet	Return for Transistor Outputs			

The serial communications port provides 4 signals: TD, RD, RTS, CTS in the modem sense. These are low-voltage signals connected via the backplane to the Power/Comms module slot.
This permits a choice of methods of connection to a computer: for example the POCO-01 Power/Comms module supplied with the starter kits provides an RS-232 interface.

Interface to Diagram:

The Slot address for all facilities is always Slot 0 for a CPDA-02.

Subslot 0: Input/Output

Register 0: Device Identifier: returns hex A522 (42274) for CPDA-02.
Register 1: Contact/NPN Inputs: bit mapped: use mask to select required input.
Register 2: Analogue Input 8: returns 0 to 1.00 (input voltage).
Register 3: Analogue Input 9: returns 0 to 1.00 (input voltage).
Note that writing (outputting) to the above registers has no effect.
Register 4: Transistor Outputs: bit mapped: use mask to select required output.
Register 5: Analog Output 8: 0 to 10.00 corresponds to output voltage.
Register 6: Analog Output 9: 0 to 10.00 corresponds to output voltage.
Register 7: Count6: medium-speed up counter attached to ISW6.
Register 8: Count7: medium-speed up counter attached to ISW7.
Register 9: CountQ: medium-speed up/down quadrature counter attached to ISW6 and ISW7.
Register 10: CountCtrl: Provides reset and hold facilities for the medium-speed counters.
Mask 1: C6 Reset: Forces Count6 to zero. Once the reset has occurred, the bit itself is reset automatically.
Mask 2: C6 Hold: Stops Count6 and holds its value. Set and reset via TERMOUT.
Mask 4: C7 Reset: Forces Count7 to zero. Once the reset has occurred, the bit itself is reset automatically.
Mask 8: C7 Hold: Stops Count7 and holds its value. Set and reset via TERMOUT.
Mask 16: CQ Reset: Forces CountQ to zero. Once the reset has occurred, the bit itself is reset automatically.
Mask 32: CQ Conditional Reset: Forces CountQ to zero when ISW6 and ISW7 are both FALSE (high). Once the reset has occurred, the bit itself is reset. This function is useful where the index signal on a quadrature encoder spans more than one step of the encoder.
Registers 11 through 60: Computer Interface: These registers can be written to by an external computer and read into the Control Diagram, or written by the Control Diagram and read by the external computer. See the Advanced Programmer's Manual for details.

Advanced Programming Capabilities

Advanced programming capabilities are accessible via subslots 1 through 6 and 255. These require advanced knowledge of computer interfacing and software. Details are provided in the AmbiLogique Advanced Programmer's Manual, but they are summarised here:

Subslot 1: Readout of Internal Signals

Reg 0 Mask 0: Signal Refnum (read/write).
Reg 1 Mask 0: Signal Value (refnum non-preincremented) (read only).
Reg 2 Mask 0: Signal Value (refnum preincremented) (read only).
| |
Reg 16 Mask 0: Signal Value (refnum preincremented) (read only).

Advanced Programming Capabilities (continued)

Subslot 2: Operating Mode and Communications Statistics

Reg 0 Mask 1:	Operating Mode: 0 = normal; 1 = stopped (read/write). This defaults to 0 (run) on power-up.
Reg 0 Mask 128:	Software Initiated Restart. Automatically cleared when restart occurs.
Reg 1 Mask 255:	Time used in processing diagram: 0 = none; 255 = full slot time allocation (read only).
Reg 2 Mask 0:	Millions of backplane transactions.
Reg 3 Mask 0:	No. of backplane transactions up to 1 million
Reg 4 Mask 0:	No. of backplane transactions in error.
Reg 5 Mask 0:	NoRep count: No Response to BRQ or BCM packet.
Reg 6 Mask 0:	Timeout count: Slave took excessive time to provide complete response.
Reg 7 Mask 0:	SentErr count: Incorrect packet sentinel detected.
Reg 8 Mask 0:	FormErr count: Format of received packet incorrect.
Reg 9 Mask 0:	CWErr count: Checkword of received packet did not compute correctly.

Subslot 3: Constants Memory (User Constants)

Reg 0 Mask 0:	Constant Refnum (read/write)
Reg 1 Mask 0:	Constant Value (refnum non-preincremented) (read/ write occasionally)
Reg 2 Mask 0:	Signal Value (refnum preincremented) (read/ write occasionally)
| |	
Reg 16 Mask 0:	Signal Value (refnum preincremented) (read/ write occasionally)

Subslot 4: Function Block Memory (User Program)

Reg 0 Mask 0:	Func Block Exec number (read/write)
Reg 1 Mask 0:	Func Block Type number (read/ write occasionally)
Reg 2 Mask 0:	Pin 0 Descriptor (read/ write occasionally)
| |	
Reg 16 Mask 0:	Pin 16 Descriptor (read/ write occasionally).

Note that Registers 1 and upwards are read-write only when the processor is in Progam mode: when in Run mode these registers are read-only.
The Function pins are masked: the signal refnum to which the pin connects is mask 4095 (hex 0x0FFF), and the pin type is mask 28672 (hex 0x7000).

Subslot 5: Reserved

Subslot 6: K-Factor Fixed-location Constants Read/Write

Reg 0 Mask 0 K-Factor Ref number (read/write)
Reg 1 Mask 0 K-Factor

Note that these K-Factors are read directly from the K-Factor Store accessed via this interface, so that a change to any K-Factor is activated immediately in the Control Diagram.
K-Factors are introduced into the Control Diagram via TERMIN blocks with sUbslot = 6.

Because K-Factors are held in flash memory, it is necessary to read out the entire set, edit the changes externally, then write the entire block back. The process of writing the first K-Factor automatically pre-erases the appropriate flash memory block.
When this occurs, the CPDA-02 switches control to a copy of the original K-factors held in RAM. This means that the process being controlled continues without interruption.
Once the new K-Factor set has been uploaded and verified, it is written into the K-Factor flash memory area. When this is complete, the PLC switches back to the flash memory and the new K-Factors control the process.
This entire process takes a fraction of a second, so it means that processes can be dynamically tuned in real time via the K-Factors.

The AmbiLogique PLC support software incorporates a special editor which permits the K-Factors to be edited and maintained. This uses a script file which can be edited so as to name each K-Factor and provide minimum, maximum and recommended values for any application.

Subslot 255: Firmware Revision Level

Reg 0 Mask 0: Firmware Revision
(Major_revision * 256) + minor_revision.
Example: Rev 3.20 => (3 * 256) + 20 = 788.
Easily decoded as a hexadecimal number:
788d = 314h => 300h + 14h => 3.20

Reg 1 Mask 0: Serial Number

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Specifications

1. Power Input:
   +14V 50 mA, +7.5V 150 mA
   This is the standard output from the
   AmbiLogique Power/Comms modules – so you don't have to worry about it.

2. Contact / NPN Transistor Digital Inputs:

Excitation voltage:	6.0 to 9.0 V
Sink current:	3.0 to 5.0 mA
Maximum Input voltage:	-1.0 to +120 V
Protection:	Blocking diode
Internal signal:	open = FALSE; closed = TRUE;
Thresholds:	5.0 V (open); 3.0 V (closed) typical

3. Analogue Inputs:

Resolution:	12 bits: 274 µV per bit
Range:	0 to 1.05 V
Input resistance:	11.1 kΩ
Total errors not exceeding:	4 bits: 1.2 mV: 0.12 % of full range
Internal signal:	0 to 1.05

4. Transistor Digital Outputs:

Max working voltage:	+ 33 Vdc
Max current:	2.0 A individually: total for all outputs not to exceed 8A
Protection:	Internal VDR

5. Analogue Outputs:

Resolution:	12 bits : 2.4 mV per bit
Range:	0 to +10 V
Internal Resistance:	100 ohms ± 1%
Max Current:	10 mA
Total errors not exceeding:	4 bits : 10 mV : 0.1 % of full range
Internal signal:	0.0 to 10.0

6. Scan Rate — 16 Hz (62.5 ms)

7. Diagram Capacity — 800 Function Blocks of any type

8. Dimensions:

Heights:	83 mm above backplane 97 mm above mounting base when assembled on to an AmbiLogique backplane on TS35 rail.
Width:	25.0 mm max
Depths:	103 mm over body 125 mm over terminals

9. Ambient temperature: -10 to +60 °C

Please Note: Some AmbiLogique products or components may carry the "AmbiLogic" trade mark from our former Australian company.

Indicators

There are 3 groups of indicators on the top panel of the CPDA-01.

Contact / NPN Input Group:
These are labelled "**ISW0**" through "**ISW7**"
The indicators are ON when the input is TRUE, i.e. switched to Return.

Analog Input Group:
These are labelled "**IAN8**" and "**IAN9**"
The indicators glow with an intensity proportional to the input voltage.

Status:
This indicator normally flashes once per second when a diagram is running. The length of the flash indicates the amount of each time slot occupied by computing the diagram. Large diagrams with lots of calculation take longer.
When the processor is stopped (typically during program upload) this indicator flashes much faster: 8 times per second.
If this indicator is not flashing, either there is no power to the processor or the processor has failed completely.

Analog Output Group:
These are labelled "**OAN8**" and "**OAN9**"
The indicators glow with an intensity proportional to the output voltage.

Transistor Output Group:
These are labelled "**OTR7**" through "**OTR0**"
These indicators are ON when the corresponding output transistor is ON.

Function Block Library

For more detail on any of these functions, a full description is displayed on the function block selector panel in the AmbiL_PLC support software.
The function block library built into the CPDA-02 with firmware 2.0 and above includes:

TERMINALS

TERMIN	Returns the state of a digital or analog input terminal.
TERMOUT	Delivers a signal to a digital or analog output terminal.

LOGIC GATES

AND	Binary AND gate
OR	Binary OR gate
XOR	Exclusive-OR gate
VOTE	Vote gate returns the number of digital inputs asserted, i.e. counts votes.
BITAND	Bitwise AND gate operates on analog values.
BITOR	Bitwise OR gate operates on analog values.
MASKIN	Returns a specific bitfield from an analog signal.
MASKOUT	Aligns and selects a specific bitfield into an analog signal.
BITASS	Assembles a number of digital signals into an analog register.
PRIORITY (new in f/ware 2.0 and above)	Accepts digital inputs numbered 1...15 and outputs the number corresponding to the highest asserted input.

Function Block Library (continued)

LATCHES & MEMORIES

LATSR	Set/Reset Latch: the Set input is edge-triggered.
LATDET	D-type Latch: on a False-True transition of the Clock input, the state of the D input is transferred to the output.

TIMERS & COUNTERS

TIMER	On a False-True transition of its Start input, outputs a count starting at the programmed time, and reducing to zero. The count decrements every PLC cycle, i.e. 16 counts per second.
CLOCK	Runs continuously counting from Period-1 down to zero, then restarting the process. Periods are in 1/16 second, as for the Timer above.
COUNT	An up/down counter with preset and clear. Edge-triggered Event input.
PREVSCAN	Returns the value of a signal at the end of the previous trip through the Control Diagram, i.e. 1/16 second ago. Useful for detecting rate of change of a signal.

ANALOG FUNCTIONS

RAMP	Adds to or subtracts from an analog signal. The step can be any analog value.
SAMPH	Sample/Hold. When the Sample input is True, the input signal is passed through to the output. When Sample is False, the output signal is held.
PREVSCAN	See under Timers & Counters.
BITASS	See under Logic Gates.

SIGNAL SELECTION

SELCT	Effectively a rotary selector switch. The Sel input determines which of the other inputs is routed to the output.
HIEST	Returns the most positive of all its input signals.
LOEST	Returns the most negative of all its input signals.
BIGST	Returns the input signal with the greatest magnitude.
SMLST	Returns the input signal with the smallest magnitude.

COMPARISON

CMPEQ	Outputs True if the two inputs are equal
CMPGT	Outputs True if the 'x' input is more positive than 'y'
CMPLT	Outputs True if 'x' is more negative than 'y'
INRANGE	Outputs True if the 'Sig' input is within the 'Hi' and 'Lo' inputs.

BASIC ARITHMETIC

ADD	Add.
SUB	Subtract.
MULT	Multiply.
DIV	Divide.
QUOT	Quotient: integer part of 'x' / 'y'
REM	Remainder: the least value left from 'x' after an integer number of 'y' have been subtracted.
RATIO	'x' * 'y' / 'z'

Function Block Library (continued)

TRIGONOMETRIC	Note that angles are expressed in revolutions, not degrees.
SINE	Sine.
COS	Cosine
TAN	Tangent
ASIN	Arc sine: returns the angle whose sine is the input.
ACOS	Arc cosine.
ATAN	Arc tangent.
LOGARITHMIC	
LOG2	Logarithm to base 2.
ALOG2	Antilogarithm to base 2.
POW	'x' to the power of 'y'

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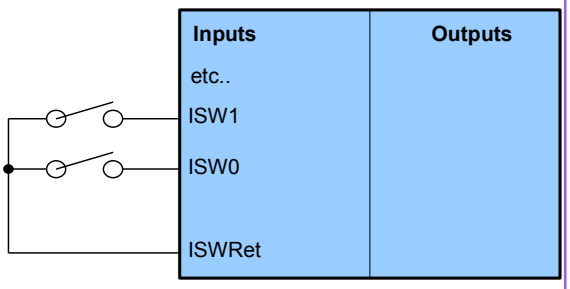
Connecting External Devices

1. Switch Inputs ISW0..7

a) Contact Input:

Wire the contact between ISW.. and ISWRet.

The input will be TRUE when the contact is closed.

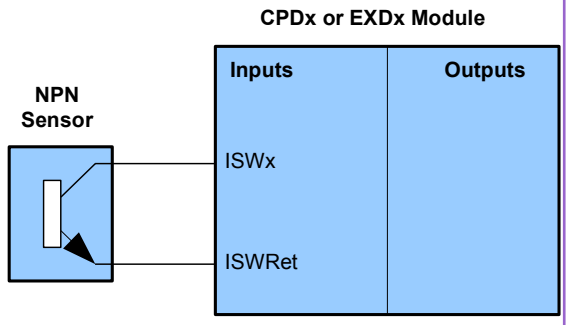


Switch Inputs

b) NPN Transistor Input:

Collector to ISW..
Emitter to ISWRet

The input will be TRUE when the transistor is ON.

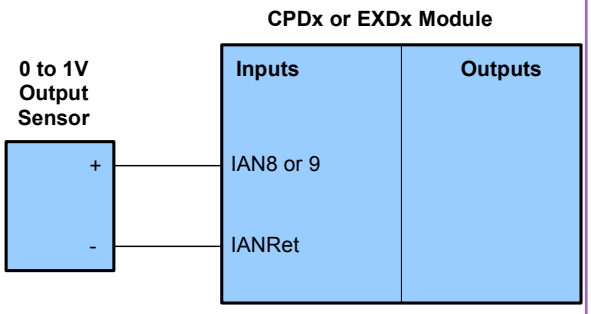


NPN Transistor Inputs

2. Analog Inputs IAN8, 9:

a) 0 to 1 V input:

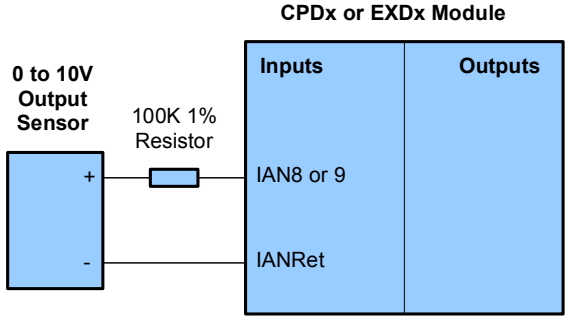
Positive to IAN8 or 9
Negative to IANRet
Remember that IANRet is not isolated from the PLC 0V line.



0-1V Analogue Inputs

b) 0 to 10 V input:

Positive to a 100 Kohm 1% resistor
Other side of the resistor to IAN8 or 9
Input resistance of IAN8 and IAN9 is 11.1 Kohm ± 0.1%.
Negative of the input to IANRet
Remember that IANRet is not isolated from the PLC 0V line.

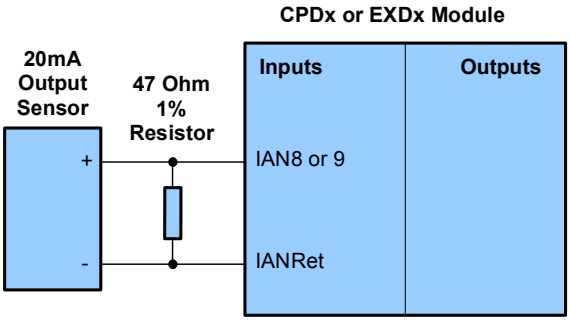


0-10V Analogue Input

3. Connecting External Devices (continued)

a) 0 to 20 mA or 4 to 20 mA input:

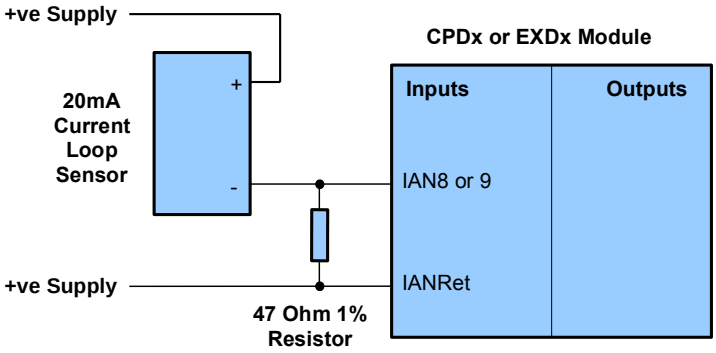
Wire a 47 ohm 1% resistor between IAN8 or 9 and IANRet.
Positive input to IAN8 or 9 (and the resistor).
Negative input to IANRet.
Remember that IANRet is not isolated from the PLC 0V line, so the PLC must be the lowest device in the loop.
In the case of 4-20 mA input, 4 mA will input 0.188 to the diagram, and 20 mA will input 0.940 to the diagram.
There is sufficient overhead on the input to allow for detection of overcurrent conditions: 22 mA gives a control diagram input of 1.034 which is within the linear input range of the CPDA or EXDA analogue inputs.



20mA Analogue Input

b) 4 to 20 mA Current Loop Sensor:

As above, a 47 ohm resistor provides the current termination.
The sensor is wired in series with the positive of the sensor supply (usually 24Vdc).
4 mA inputs 0.188 into the control diagram;
20 mA inputs 0.940 into the diagram.



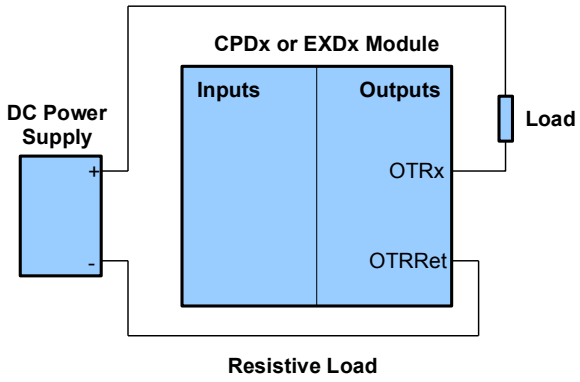
20mA Current Loop Sensor Input

Connecting External Devices (continued)

4. Transistor Outputs OTR0..7:

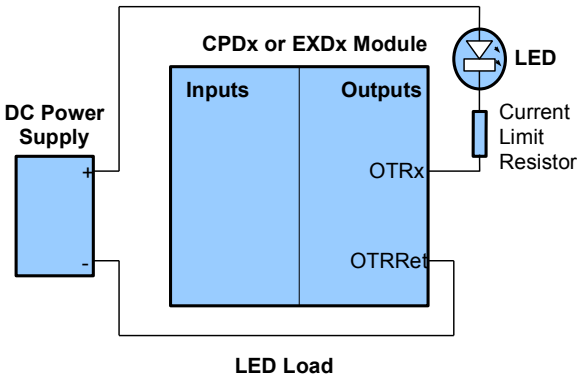
a) Resistive Loads:

Negative terminal of the power supply feeding the load to OTRRet.
Positive terminal of the load to the positive terminal of the power supply.
Negative terminal of the load to OTR0..7 as required.
Note that OTRRet is connected to the PLC 0V line.



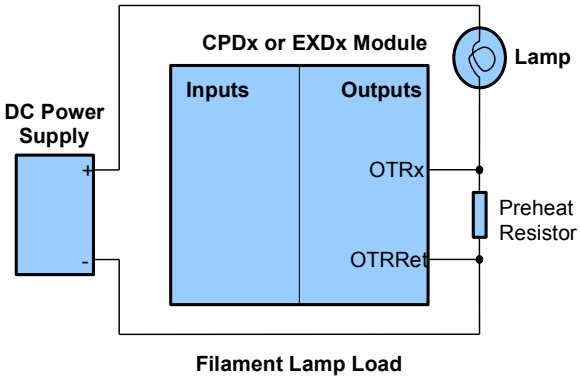
b) LEDs:

Determine whether the LED is fitted with a current limiting circuit.
Most LEDs are not, and will need a current limiting resistor wired in series with them.



c) Filament Lamps:

The problem with filament lamps is the extremely low resistance when cold, giving rise to a huge current surge when switched on. One approach is to put a current limiting resistor in series with the lamp - the power supply voltage then needs to be greater than the lamp voltage.

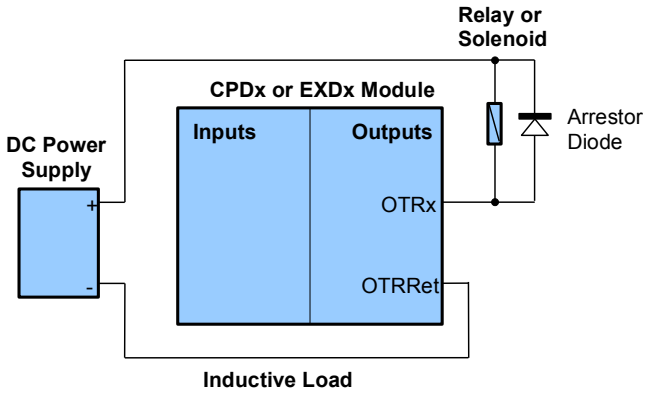


An alternative approach is to shunt the switching device with a preheat resistor whose value is such that the filament is just at the glow point when the lamp is switched off.
This approach can greatly increase lamp life where lamps are switched on and off frequently, e.g. where a lamp is flashed as a warning.

Connecting External Devices (continued)

d) Relays and Solenoids:

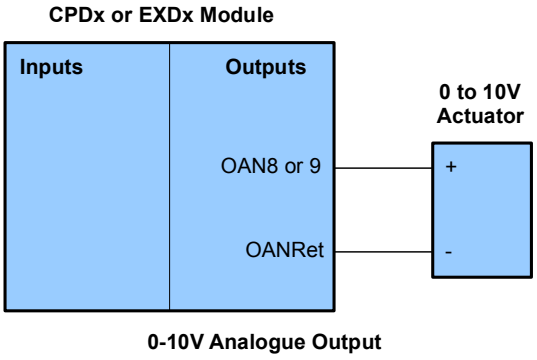
Inductive loads such as relays and solenoids normally need arrestor diodes across them to protect the switching element. AmbiLogique transistor outputs have VDR protection so that the diodes are not strictly necessary, unless the load is being switched frequently. However, fitting the diodes will reduce the voltage spikes associated with switching off inductive loads, and improve EMC performance.



5. Analogue Outputs OAN 8 and 9:

a) Voltage Output (0 to 10 V):

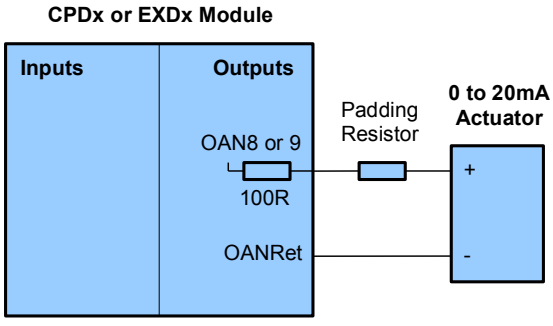
The OAN8 and OAN9 outputs have an internal resistance of 100 ohms. If the load has a significant resistance, the output voltage will be less than expected.
Most 0-to-10 V devices have input resistances greater than 100 Kohms, so the loading error will be less than 0.1% .



0-10V Analogue Output

b) Current Output (0 to 20 mA):

The total circuit resistance including loads, the internal resistance of 100 ohms, and the padding resistor needs to total 500 ohms.
An output value of 10.0 from the diagram will produce 20 mA.
An output value of 2.0 will produce 4 mA.
For a simpler and better controlled 0-20 or 4-20 mA output scheme, see the data sheet for the EXDA-4201 Expansion Module.



0-20mA Analogue Output

A Much Better Idea : Logical : Unique

AmbiLogique

Electronic Controllers

WARNING
SAFETY-CRITICAL SYSTEMS

A Safety-Critical system is a system whose failure or malfunction could cause death, significant injury or loss of property.

AmbiLogique products incorporate electronic hardware and software, both of which carry a remote but real possibility of failure. AMBILOGIQUE DOES NOT WARRANT, CLAIM OR REPRESENT THAT ITS PRODUCTS ARE INFALLIBLE.

It is therefore THE RESPONSIBILITY OF THE DESIGNER of any safety-critical system which incorporates AmbiLogique products to ensure that:-

1. The system is designed so that any failure of an AmbiLogique component will not cause death, injury or loss of property.
2. The system incorporates independent monitoring means which detect the failure of any of the electronic control elements.
3. The system has alternative and independent means of control which enable it to be controlled and shut down in an orderly manner.
4. Any and all other industry-specific safety requirements are fully implemented.

Revision History:

R 0.0	2016-01-21	Initial issue – update on CPDA-01 data sheet.
R 0.1	2020-02-03	Contact details updated.
R 0.2	2023-08-22	Software Reset added.
R 2.0	2024-09-19	Computer Interface registers increased from 16 to 50 in f/ware 2.0 and above. Priority gate added.